REMARKS/ARGUMENTS

Claims 1-23 are presently active in this case. Applicant has amended Claims 1-5, 8-12, and 15-23 and canceled Claims 24-26 without prejudice or disclaimer. Support for the amendments can be found at least at page 8, lines 14-17, page 8, line 34-page 9, line 3, page 9, lines 27-33, and pages 11, lines 9-18 of the specification. No new matter has been added.

In the Official Action, Claims 1-26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kato, et al. (U.S. Patent No. 6,070,205, herein "Kato") in view of Kenny (U.S. Patent No. 6,393,506).

The Official Action asserts that Kato discloses all of the Applicant's claim limitations with the exception of a data bus divided for transferring data concurrently. The Official Action points out that Kato does not teach or suggest that "the data bus is divided and through each of which data is transferred concurrently."[1] The Office Action cites Kenny as disclosing this more detailed aspect of the Applicant's invention.

Applicant respectfully traverses the rejection of Claims 1-23.

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), each of three requirements must be demonstrated. First, Kato in view of Kenny, in combination, must teach or suggest each and every element recited in the claims.[2] Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention.[3] Third, a reasonable probability of success must exist with respect to

[1] See Office Action of July 29, 2003, page 3.

[2] See MPEP § 2143.

[3] See id.

the proposed combination relied upon in the rejection.[4]

Amended Claim 1 recites a data transfer control circuit for carrying out data transfer by using a plurality of bus masters comprising, *inter alia*, a data bus connected to a peripheral apparatus, the data bus comprising a plurality of unit data buses, each of which transfers data concurrently. A plurality of bus masters are configured to send a request signal requesting a use of each of the unit data buses and to use the unit data buses requested when a request is granted. The request signal has a data field comprising a plurality of bits, each of the plurality of bits corresponding to a respective one of the unit data buses.

Kato relates to single-chip processor systems having a plurality of bus masters and bus arbitration mechanisms for arbitrating common bus access among bus masters.[5] Kenny relates to a system and method for coordinating the transfer of digital data between functional modules in a computer system.[6]

Kenny does not teach or suggest a data bus connected to a peripheral apparatus, the data bus comprising a plurality of unit data buses, each of which transfers data concurrently, as recited in Claim 1 as amended. In Kenny, "[e]ach virtual channel represents a timeslice on the bus and is owned by a separate master/slave pair, thereby permitting multiple master/slave pairs to have concurrent ownership of the single data bus."[7] Accordingly, only one virtual channel is used, i.e., only one virtual channel uses the data bus, at any given time.[8] Nowhere does Kenny teach or disclose a data bus composed of a plurality of unit data buses, each of which transfers data concurrently, as recited in Claim 1 as amended.

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[4] See id.

[5] See Fig. 4 of Kato.

[6] See Fig. 1 of Kenny.

[7] Kato, col. 2, lines 59-63 (emphasis added).

[8] See signals E1, E2, and E3 in Fig 9B, together with accompanying description at col. 10, lines 3-42.

Moreover, neither Kato nor Kenny discloses or suggests a request signal that has a data field comprising a plurality of bits, each of the plurality of bits corresponding to one of the unit data buses, as recited in Claim 1 as amended. Conversely, in Kato, each request signal corresponds to only one bus. In other words, "[a] first bus interface controller asserts [a] first bus request signal until it receives [a] first bus grant signal from [a] first bus arbitrator"[9] and "[a] second bus interface controller asserts [a] second bus request signal until it receives [a] second bus grant signal from [a] second bus arbitrator"[10] Then, for example, a "CPU is allowed to access the second bus from the time it receives the second sub grant signal . . ."[11] Nowhere does Kato teach or suggest a request signal that has a data field comprising a plurality of bits, each of the plurality of bits corresponding to one of the unit data buses, as recited in Claim 1 as amended.

Likewise, Kenny does not cure the deficiencies of Kato in this regard. For example, even assuming Kenny could properly be combinable with Kato, which Applicant disputes, Kenny does not teach or suggest at least a request signal that has a data field comprising a plurality of bits, each of the plurality of bits corresponding to one of the unit data buses, as recited in Claim 1 as amended.

Accordingly, Applicant respectfully submits that Claim 1 is patentable over the cited combination of references. Independent Claims 8, 15, and 21-23, although of different statutory class and/or of different scope, include recitations similar to those discussed above in relation to Claim 1. Similarly, Claims 2-7, 9-14, and 16-20 depend from Claims 1, 8, or 15 and are likewise allowable.

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[9] Kato, col. 11, lines 56-59.

[10] Kato, col. 11, line 67-col. 12, line 2.

[11] Kato, col. 12, lines 2-4.

Accordingly, in view of the foregoing amendments and remarks, it is respectfully submitted that the present application, including Claims 1-23, is patentably distinguished over the prior art, is in condition for allowance, and such action is respectfully requested at an early date.

Respectfully submitted,

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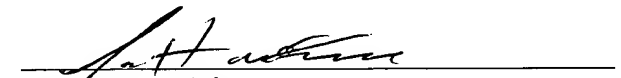

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